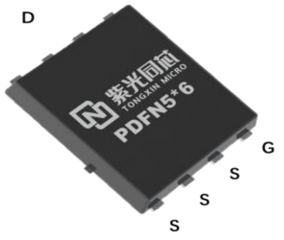
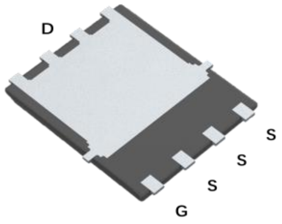
THF1D3S40LKN2A
Datasheet

Product Summary

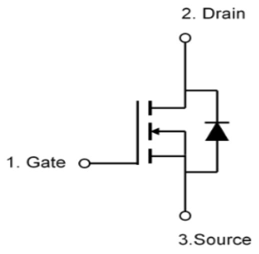
Parameter	Value	Unit
V_{DS}	40	V
$V_{GS(th)\_Typ}$	1.7	V
I_D (@ V_{GS} = 10V) (1)	207	A
$R_{DS(ON)\_Typ}$ (@ V_{GS} = 10V)	1.1	mΩ





Features

- Fast Switching
- Very low on-resistance
- Enhancement mode
- 100% Avalache Tested
- 100% ΔVds Tested
- Halogen-free and RoHS-compliant



Typical Applications

- Load Switch
- PWM Application
- Power Management

RoHS PB Pb-free HF Halogen-free

Product Validation

- Qualified for Automotive Applications. Product validation according to AEC-Q101

Ordering Information

Device	Package	Quantity of Pins	Marking	MSL	T_J (°C)
THF1D3S40LKN2A	PDFN5x6-8L	8	1D3S40LKN	1	-55 to 175

Absolute Maximum Ratings (@ T_A = 25°C unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DS}	40	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (1)	T_C = 25°C	I_D	207	A
	T_C = 100°C		146	A
Pulsed Drain Current (2)		I_{DM}	828	A
Avalanche Current (3)		I_{AS}	73	A
Avalanche Energy (3)		E_{AS}	266	mJ
Power Dissipation (4)	T_C = 25°C	P_D	104	W
	T_C = 100°C		52	W
Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

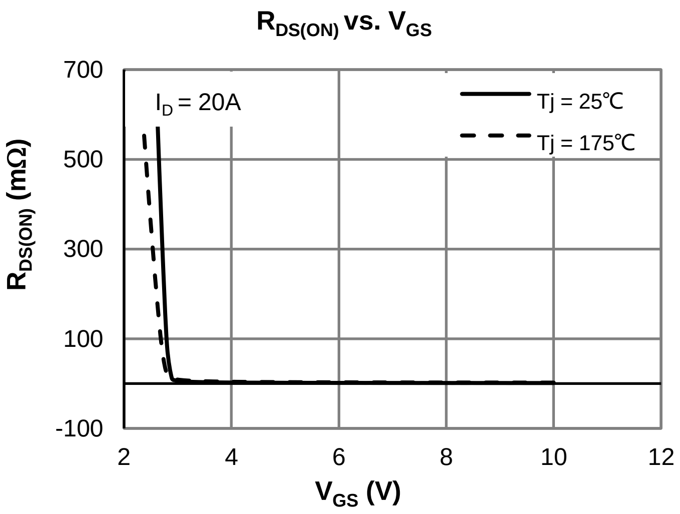


Figure 1: $R_{DS(ON)}$ VS. V_{GS}

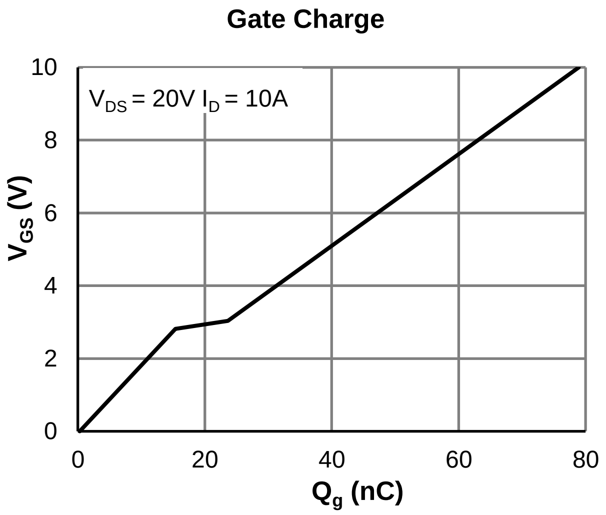


Figure 2: Gate Charge Curve

Electrical Characteristics (@ T_J = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250μA, V_{GS} = 0V	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V	-	-	1.0	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.7	2.5	V
Static Drain-Source ON-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 50A	-	1.1	1.3	mΩ
		V_{GS} = 4.5V, I_D = 50A	-	2.0	2.4	
Diode Forward Voltage	V_{SD}	I_S = 50A, V_{GS} = 0V	-	0.8	1.0	V
Diode Continuous Current	I_S	T_C = 25°C	-	-	138	A
DYNAMIC PARAMETERS $^{(5)}$						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz	-	6042	-	pF
Output Capacitance	C_{oss}		-	3217	-	pF
Reverse Transfer Capacitance	C_{rss}		-	60.8	-	pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS}= 0V, f = 1MHz	-	1.1	-	Ω
SWITCHING PARAMETERS $^{(5)}$						
Total Gate Charge (@ V_{GS} = 10V)	Q_g	V_{GS} = 0 to 10V V_{DS} = 20V, I_D = 50A	-	78	-	nC
Gate Source Charge	Q_{gs}		-	14.0	-	nC
Gate Drain Charge	Q_{gd}		-	8.0	-	nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS} = 10V, V_{DS} = 20V I_D = 50A, R_{GEN} = 1.6Ω	-	8.0	-	ns
Turn-On Rise Time	t_r		-	9	-	ns
Turn-Off DelayTime	$t_{D(off)}$		-	33	-	ns
Turn-Off Fall Time	t_f		-	12	-	ns
Body Diode Reverse Recovery Time	t_{rr}	I_F = 50A, dI_F/dt = 100A/μs	-	42	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	68.0	-	nC

Thermal Performance

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	45	54	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.2	1.4	°C/W

Notes:

1. *Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.*
2. *This single-pulse measurement was taken under T_{J_Max} .*
3. *This single-pulse measurement was taken under the following condition [L = 0.1mH, V_{GS} = 10V, V_{DS} = 40V] while its value is limited by T_{J_Max} .*
4. *The power dissipation P_D is based on T_{J_Max} .*
5. *This value is guaranteed by design hence it is not included in the production test.*

Typical Electrical & Thermal Characteristics

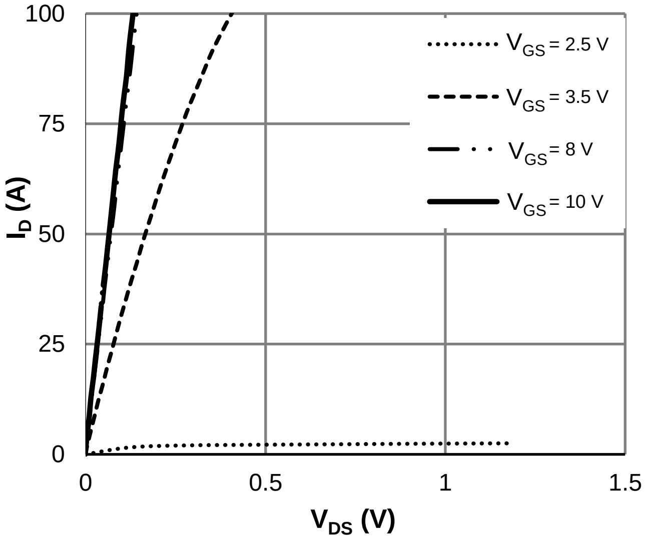


Figure 3: Saturation Characteristics

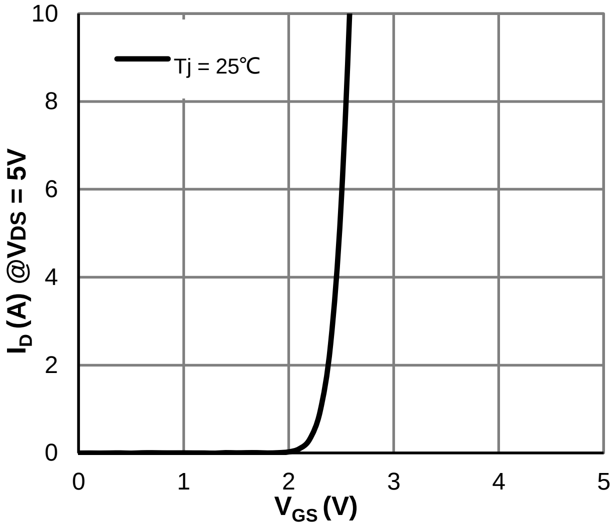


Figure 4: Transfer Characteristics

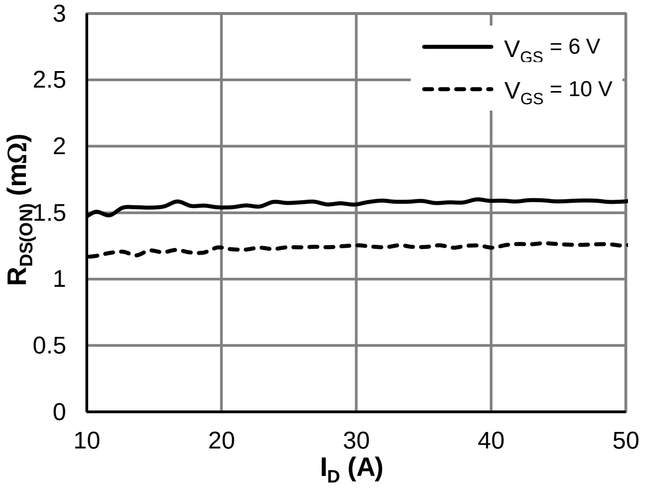


Figure 5: RDS(ON) vs. Drain Current

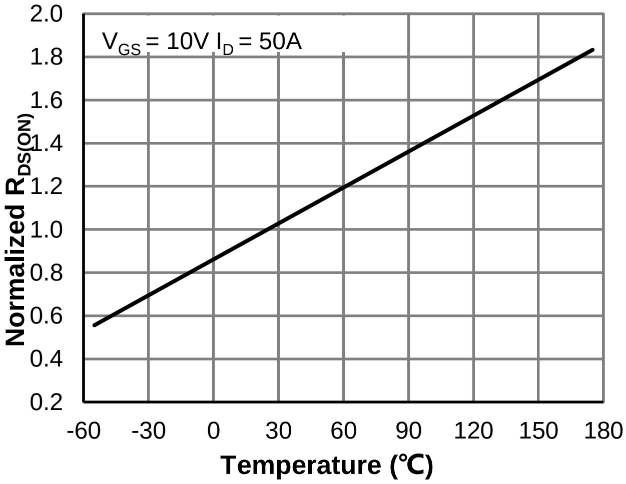


Figure 6: RDS(ON) vs. Junction Temperature

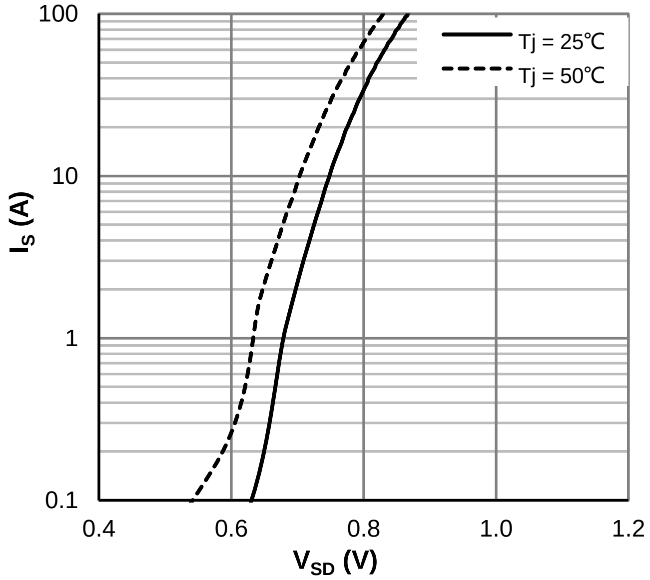


Figure 7: Body-Diode Characteristics

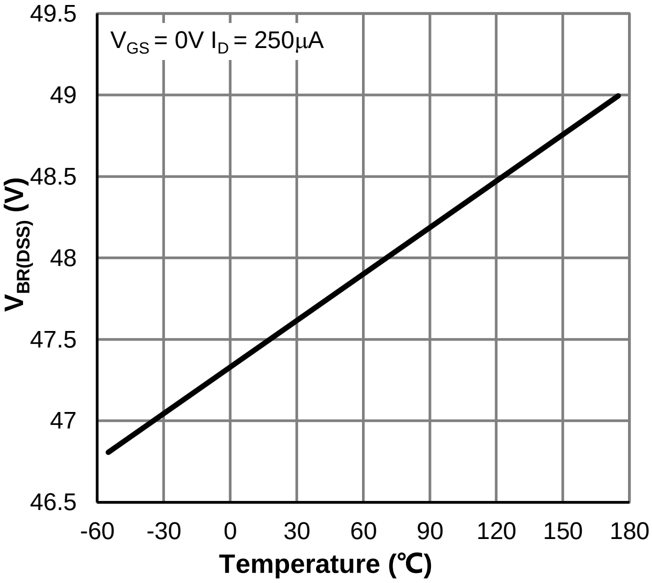


Figure 8: $V_{BR(DSS)}$ vs. Junction Temperature

Typical Electrical & Thermal Characteristics

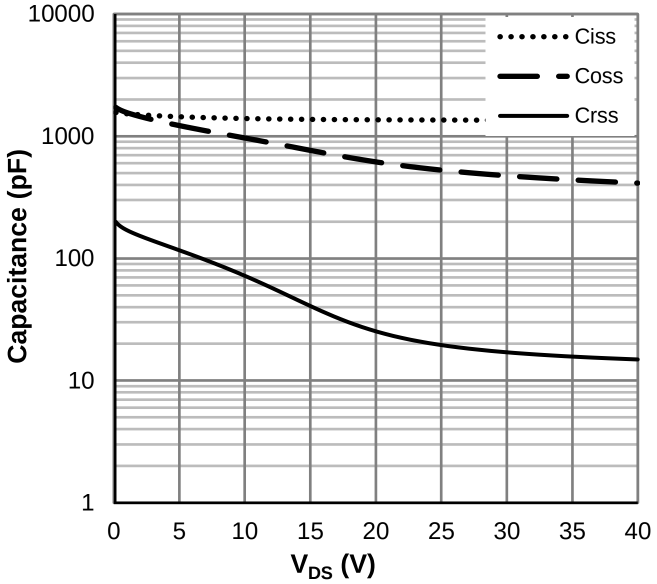


Figure 9: Capacitance Characteristics

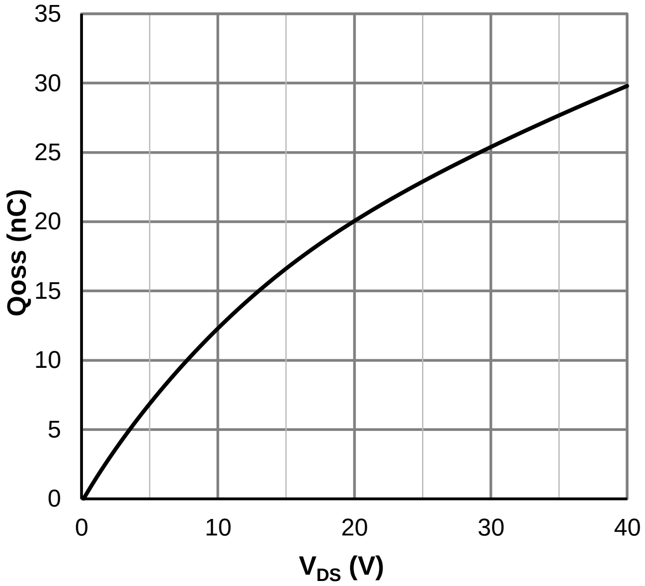


Figure 10: Coss Stored Energy

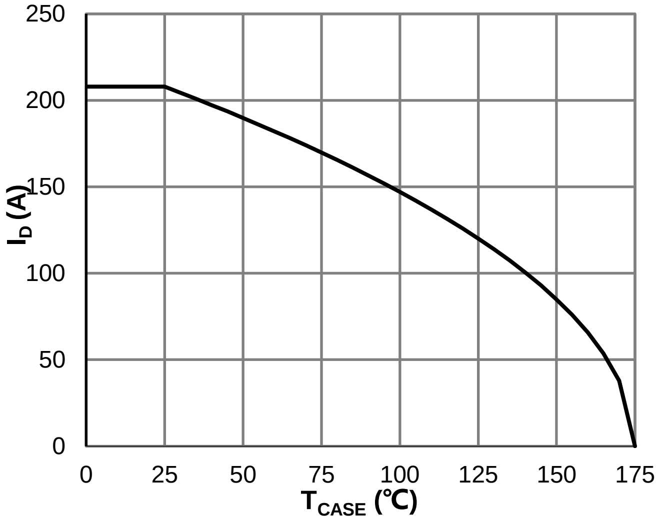


Figure 11: Current De-rating

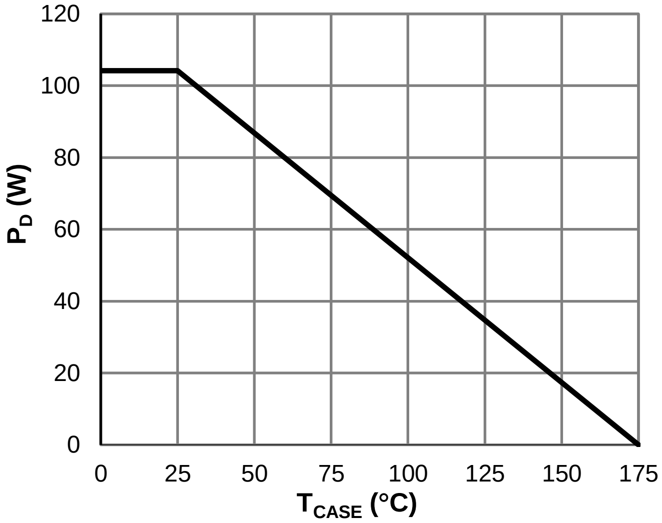


Figure 12: Power De-rating

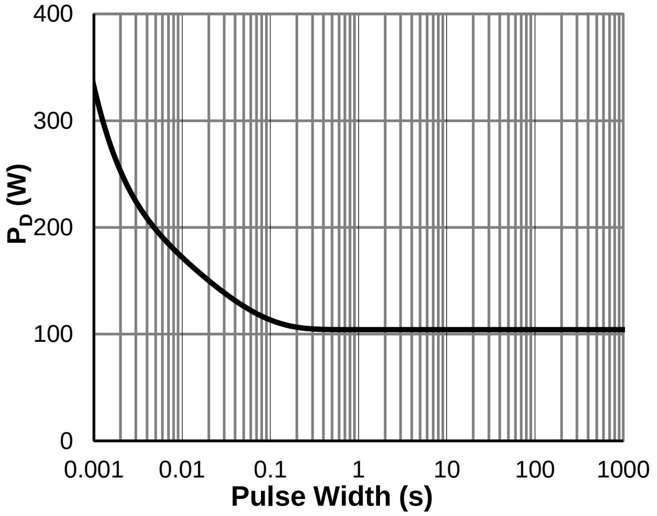


Figure 13: Single Pulse Power Rating, Junction-to-Case

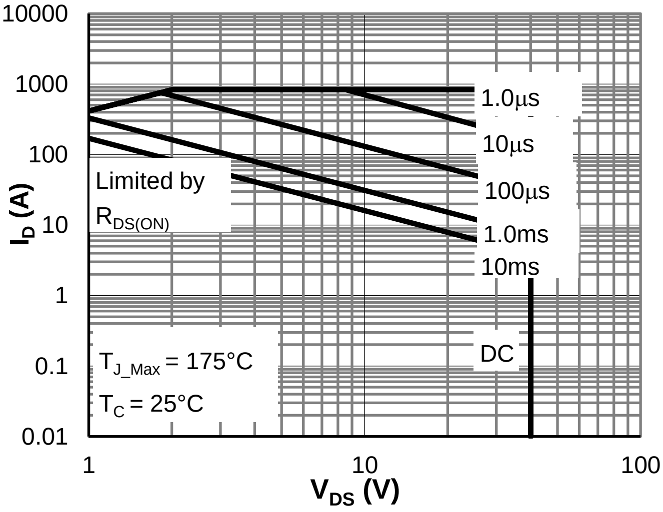


Figure 14: Maximum Safe Operating Area

Typical Electrical & Thermal Characteristics

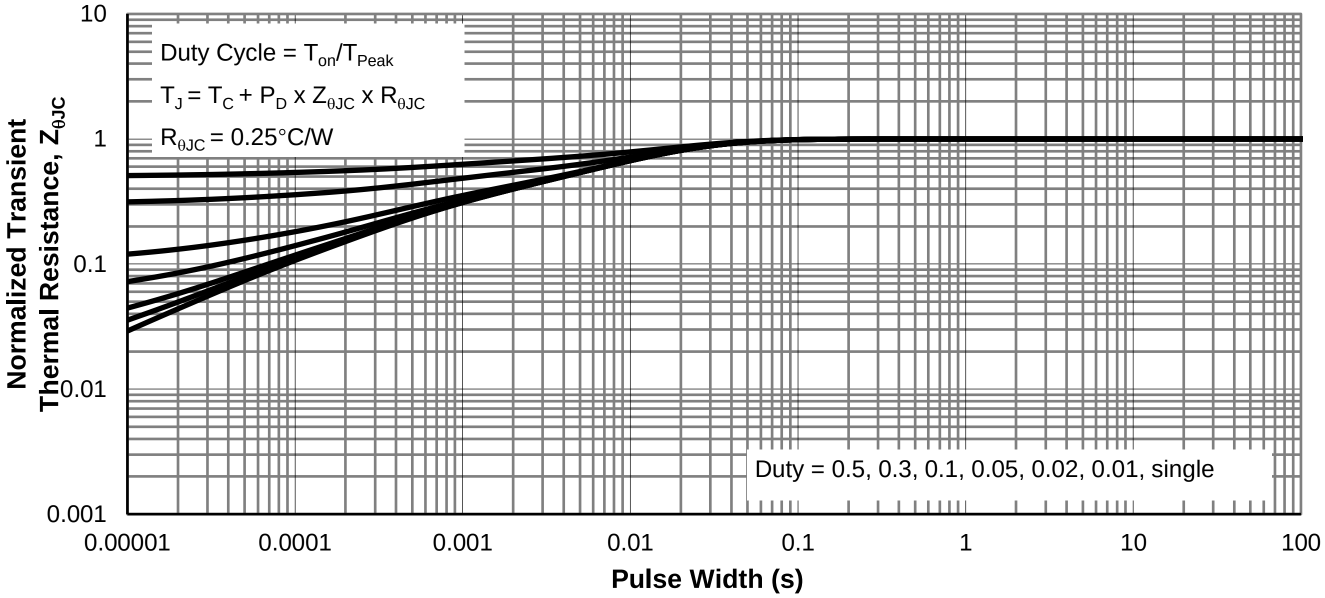
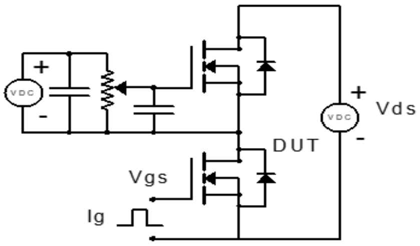
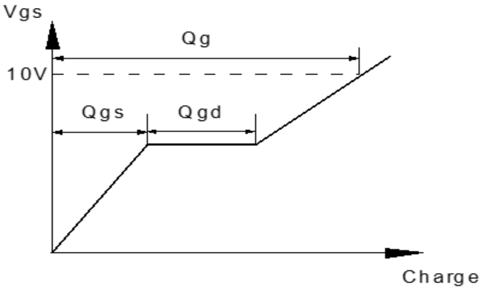


Figure 15: Normalized Maximum Transient Thermal Impedance

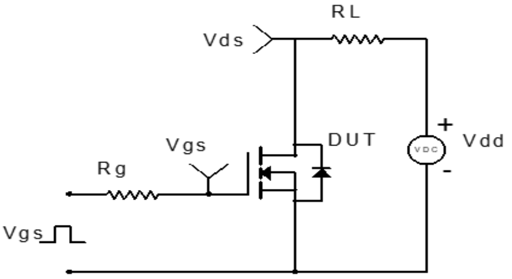
Test Condition

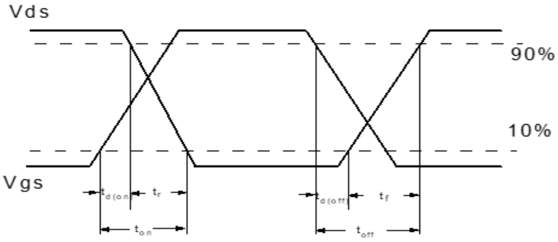
Gate Charge Test Circuit & Wave Form



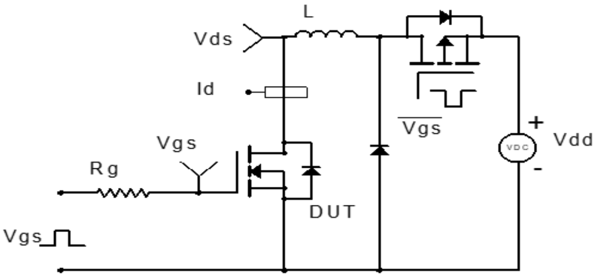


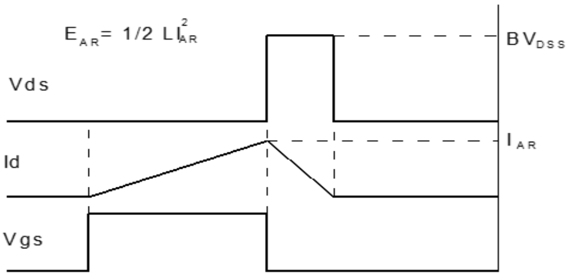
Resistive Switching Test Circuit & Wave Form



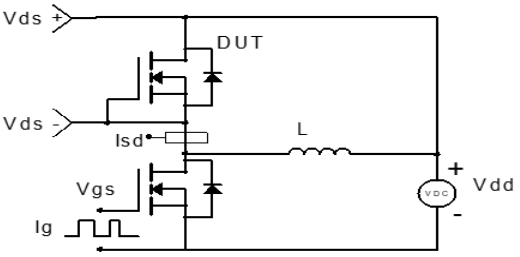


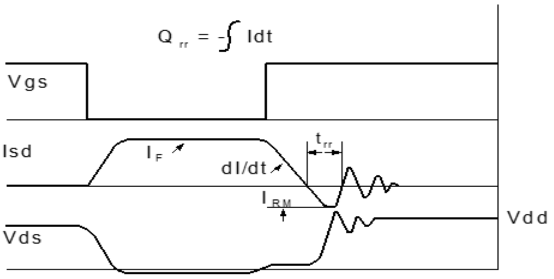
Unclamped Inductive Switching(UIS)





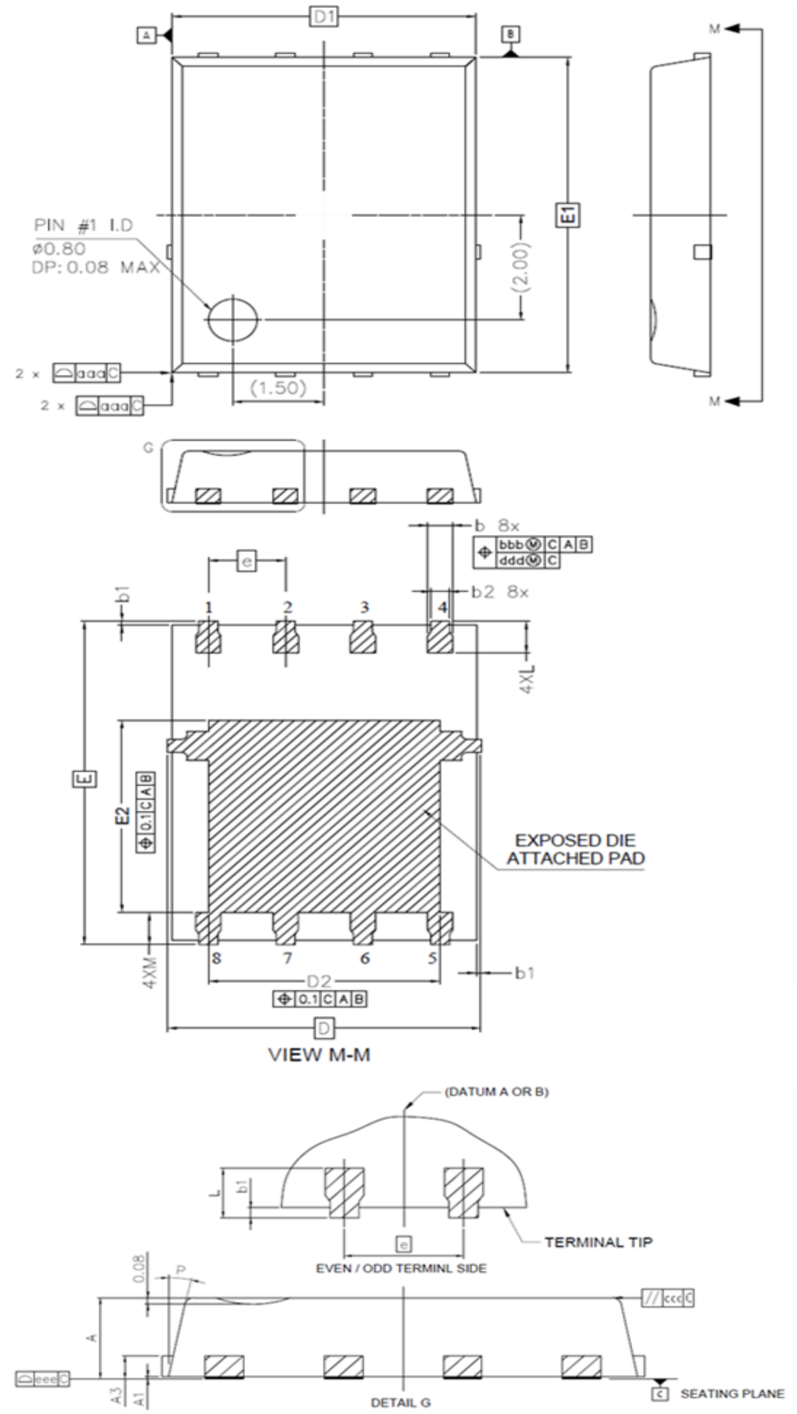
Diode Recovery Test Curcuit & Wave Form





Package Outlines

Package Drawing PDFN5*6



DIM	MILLIMETERS	
	MIN	MAX
A	0.95	1.05
A1	0.00	0.05
A3	0.25 REF	
b	0.31	0.51
b1	0.03	0.13
b2	0.21	0.41
D	5.15 BSC	
D1	5.00 BSC	
D2	3.70	3.90
E	6.15 BSC	
E1	6.00 BSC	
E2	3.56	3.76
e	1.27 BSC	
L	0.51	0.71
M	0.51	0.71
P	10°	12°
aaa	0.10	
bbb	0.10	
ccc	0.10	
ddd	0.05	
eee	0.08	

Contact US

Home Page: https://www.tsinghuaic.com
Address: 106A F/1, Building B-1, Zhongguancun Dongsheng Technology Park Northern Territory,
No.66 Xixiaokou Road, Haidian District, Beijing
Phone: +86-10-82351818-310

Business1
Phone: +86-10-82351818-376
E-mail: sales2@tsinghuaic.com

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Version	Change Description
V1.0	initial version

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